Quad-SHARCs AD14060/AD14160
480-MFLOP, Single Package Multiprocessor

The **AD14060** Quad-SHARC is a first generation (CQFP) DSP multiprocessor. Using high-density packaging techniques, the module fits four SHARCs in approximately 30% of the space required using discrete packages.

The **AD14160** Quad-SHARC Ceramic Ball Grid Array (CBGA) puts the power of the first generation AD14060 (CQFP) DSP multiprocessor into a very high density ball grid array package, the module fits four SHARCs in approximately 30% of the space required using discrete packages; now with additional link and serial I/O pinned out, beyond that from the CQFP package.

The core of the multiprocessors is the ADSP-21060 DSP Microcomputer. The AD14060/ AD14160 modules have the highest performance-density and lowest cost-performance ratios of any multiprocessors in their class. They are ideal for applications requiring higher levels of performance and/or functionality per unit area.

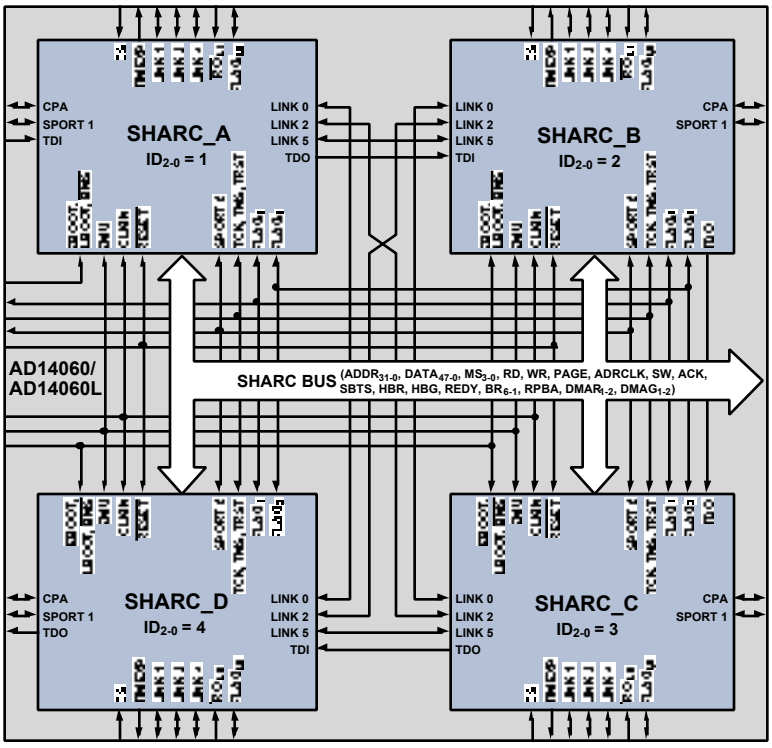
The AD14060/AD14160 take advantage of the built-in multiprocessing features of the ADSP-21060, to achieve 480 peak MFLOPS with a single chip type, in a single package. The on-chip SRAM of the DSPs provides 16 Mbits of on-module shared SRAM. The complete shared bus (48-bit data, 32-address) is also brought off-module for interfacing with expansion memory and/or other peripherals.

Applications

Multi-SHARC designs with tight area/volume constraints, such as large array and image processors, smart missiles, avionics, and others will benefit. The AD14060/AD14160 are available as both industrial and MIL-SMD grade parts in 5V (AD14060/AD14160) or 3.3V (AD14060L/AD14160L) versions.

Competition

With 480 MFLOPS of throughput, the AD14060/AD14160 have no competition. TI's Dual C40 MCM provides a similar function, but delivers only 80 MFLOPS in a significantly larger package, and roughly equivalent cost. The Quad-SHARC AD14060/AD14160 is targeted to be priced such that users can take advantage of system cost advantages of using MCMs.



AD14060 Functional Block Diagram

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Quad-SHARCs AD14060/AD14160

Development Tools

Both the AD14060 and AD14160 are supported with a complete set of software and hardware development tools, including an ADSP-21061 EZ-KIT Lite, and development software.

Features

- ADSP-21060 core processor (. . . x4)
- 480 MFLOPS Peak, 320 MFLOPS sustained
- 25 ns instruction rate, single-cycle instruction execution - each of 4 processors
- 16 Mbit shared SRAM (internal to SHARC's)
- 4 gigawords addressable off - module memory
- 48-bit shared memory bus, 48-bit data bus
- Full 32-bit address bus
- Interrupts, flag pins, and timers are also avail able as I/O
- 32-Bit single precision and 40-Bit extended precision IEEE floating-point data formats, or 32-Bit fixed-point data format
- User configurable boot modes, bus priority, and other features with control lines
- IEEE JTAG standard 1149.1 test access port and on-chip emulation

AD14060

– Twelve 40 Mbyte/s link ports (3 per SHARC) accessible to/from the outside world
– Four link ports connected internally in a ring configuration
– Four 40 Mbit/s independent serial ports (one from each SHARC)
– One 40 Mbit/s common serial port
– Ceramic quad flat pack with enhanced I/O
– Low-profile 2.05" 308 lead ceramic quad flat pack package

AD14160

– Sixteen 40 Mbyte/s link ports (per SHARC) accessible to/from the outside world
– Eight link ports connected internally in ring configuration
– Eight 40 Mbit/s independent serial ports (two from each SHARC) available from outside
– Ceramic ball grid array QUAD-SHARC with enhanced I/O
– Low-profile 1.85" ceramic ball grid array package

For any further inquiries, please contact MCP Marketing in Greensboro, NC at 336-668-9511

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